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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06F 12/14, 12/06, G11C 8/00, G07F 17/34 — A1

(11) International Publication Number: WO 96/24900

(43) International Publication Date: 15 August 1996 (15.08.96)

(21) International Application Number: PCT/AU96/00062

(22) International Filing Date: 8 February 1996 (08.02.96)

(30) Priority Data:
PN 1054 10 February 1995 (10.02.95) AU

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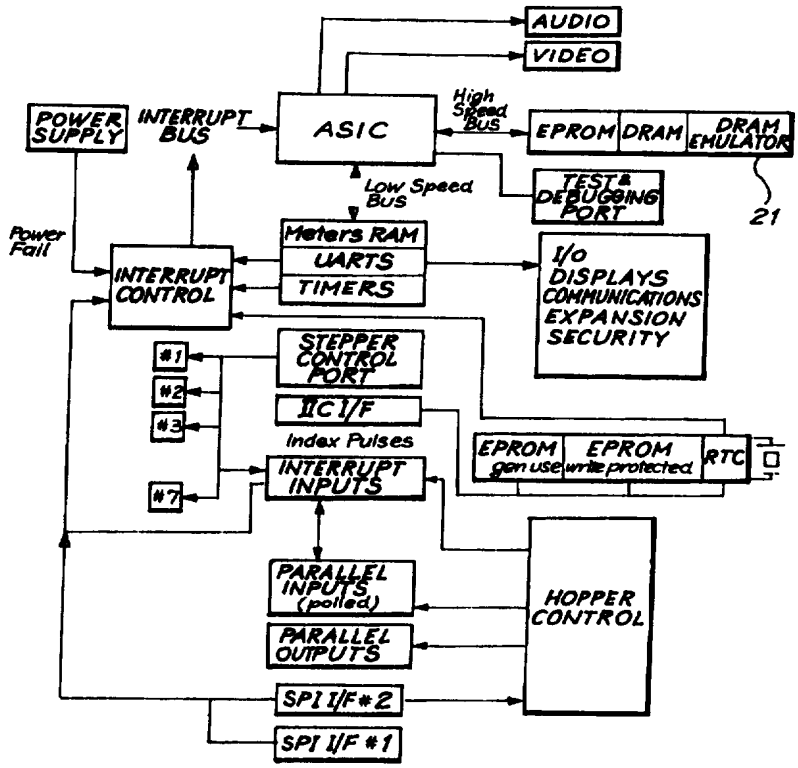
(81) Designated States: AU, DE, NZ, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: DRAM EMULATOR

(57) Abstract

A dynamic RAM emulator is provided which avoids the need of having code running in DRAM in those regulatory environments where such an arrangement is not permitted. In order to assure high performance the architecture includes electronics that simulate the DRAM using very fast bipolar PROMS. The DRAM emulator (21) is read only and can provide from 256 to 1024 32 bit words. During the DRAM cycle the multiplexed address is latched by the DRAM emulator and compared to the selected address. When the emulator is addressed the PROM is enabled (O/E) and the respective DRAM output enable (DRAM OE0 or DRAM OE1) inhibited.



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DRAM EMULATOR

Introduction

The present invention relates generally to slot machines and in particular the invention provides an improved memory system for use within a slot machine.

Regulatory authorities charged with the responsibility of ensuring that gaming machines are operated fairly and are, as far as possible, immune to fraudulent operation have become increasingly stringent in recent years in order to stamp out undesirable practices. In the process, some of these authorities have introduced rules for the design of gaming machines which attempt to prevent the machine from being operated in any manner other than that in which it was intended to operate. One such rule which some authorities have imposed is that programmes controlling the operation of a slot machine cannot run in RAM.

This presents a particular problem where the designer of a gaming machine such as a video slot machine wishes to use dynamic RAM to provide the speed required for video manipulation in this type of machine. it is also a problem when the processor selected to control a slot machine is of a type which is designed only to operate with dynamic RAM..

Summary of the Invention

According to a first aspect the present invention consists in a dynamic RAM emulator comprising a block of addressable memory and address control means arranged to address a selected word within the block. the address means including row and column latches for demultiplexing and latching a multiplexed address asserted on an address bus of a processor or a decoded memory selection signal derived from the multiplexed address, a data output arranged to be connected to a data bus of the processor and control logic to control latching of the address or memory selection signal, and enabling of the data output, said control logic also being arranged to override a data bus output enable of the processor and to enable or disable outputs of other memory devices connected to the data bus in accordance with the address latched in the address latch.

According to a second aspect, the present invention consists in a slot machine comprising game playing means and control means wherein the control means includes memory means incorporating the dynamic RAM emulator as hereinbefore described.

Brief Description of the Drawings

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 schematically illustrates the electrical configuration of a slot machine using an embodiment of the present invention;

Figure 2 is a block diagram of a first embodiment of a dynamic RAM emulator made in accordance with the present invention; and

Figure 3 is a block schematic of a second embodiment of a dynamic RAM emulator made in accordance with the present invention.

Detailed Description of the Embodiments

Embodiments of the invention will be described with reference to a gaming machine, the electrical configuration of which is illustrated in Figure 1. This machine makes use of an Application Specific Integrated Circuit (ASIC) containing a RISC processor which interconnects as shown in Figure 1.

A large majority of the functions of the gaming machine control system are built into the ASIC integrated circuit which provides:

- A 32 bits RISC processor
- Dynamic RAM Controller
- VGA resolution video controller along with 12 bit video DAC'S
- Stereo eight voices sound generation
- System glue logic, eg. Chip Enable lines and Wait State generation
- Interrupt controller
- Clock dividers

The processor connects to three system buses:

- A high speed (16 MHZ), 32 bit bus
- A low speed, 8 bit, I/O bus
- The Interrupt Bus

These buses are isolated by data and address latches. The high speed 32 bit bus is used to interface with the CPU memory, of which three types are used:

- EPROM
- DRAM
- DRAM EMULATOR 21

The ASIC processor is designed to run very quickly from Dynamic Memory using the "page mode" of the DRAM. The Device can interface to a maximum of 4 Mbytes of DRAM.

The DRAM contains the screen data with the result that part of the bandwidth of the system is lost while transferring video data to the DAC's.

Certain regulatory authorities currently do not approve the concept of having code running in DRAM. In order to assure top performance for a VGA system the architecture includes electronics that simulate the DRAM using very fast bipolar PROMS. The DRAM emulator 21 is read only and can provide from 256 to 1024 32 bit words.

Another reason to use the DRAM Emulator 21 is that the interrupt system in the ASIC processor is implemented in a way that requires at least one instruction per interrupt in DRAM. This causes problems with those authorities that do not allow machines having code running in DRAM.

Gaming jurisdictional bodies may require that no CPU code be executed from RAM. However, microprocessors are often designed so that an interrupt causes execution to commence in the RAM space. In particular the ASIC processor is designed to use dynamic RAM and the interrupt vector is intended to be located in the DRAM space. The instruction executed is usually a jump back to a location in EPROM, but even this may not be allowed by the authorities. The DRAM emulator 21 is designed to map high speed PROM into the address space occupied by the interrupt vector table to ensure acceptable performance of machines running animation on high resolution screens.

The system has 1 Mbyte of dynamic RAM as standard, with provision for an optional extra bank of 1 Mbyte.

The system implements the emulation of normal DRAM with high speed (25 nsec) bipolar PROM. The circuit is loaded only in those markets that do not allow to run code from DRAM. The DRAM Emulator 21 can provide from 256 to 1024 32 bit words of PROM.

It has been estimated that with the usage of the DRAM emulator 21, the performance will be increased by 30% over an EPROM equivalent.

A CGA system should run from normal EPROM with 12 MHZ clock with excellent animation.

Referring to Figure 2, during the DRAM Cycle the multiplexed address is latched by the DRAM emulator 21 in transparent latches 22,23

and compared in control logic 24 to the selected address, which for the interrupt vectors is page zero (1K words). When page zero is addressed the PROM is enabled (O/E) and the respective DRAM output enable (DRAM OE0 or DRAM OE1) is inhibited. This latched address also supplies a demultiplexed address to the PROMs.

The EMUL-FITTED signal enables or disables the DRAM emulator. When disabled, the entire memory space is connected to DRAM, whereas when enabled the DRAM emulator PROM is mapped to page 0.

The ASIC processor has 4 CAS outputs, CAS[3:0], which are used to control the individual bytes making up each 32 bit word. Only one of these CAS lines is required to latch the address, as on an instruction fetch all 4 lines are asserted.

Referring to Figure 3 a second embodiment is illustrated which provides only the minimum requirement to implement the invention where only vectors are stored in the emulator memory. In this embodiment only a fixed jump relative instruction is stored in the Emulator memory providing a jump to another vector table in the machine's EPROM address space. Thus all instructions are identical and only 1 word of storage is needed for all locations. This is implemented as simple logic buffers 26 with hard wired inputs 25.

Latched addresses as such are not required except for the control logic 27 which decides whether or not to enable the DRAM Emulator. Only the decoded results of the row and column addresses indicating an address within the DRAM emulator address range need be latched, but not the actual addresses themselves.

In an extended version of the embodiment of Figure 3 an extra input is provided to the control logic which disables the on board DRAM emulator and instead causes the control logic to select an external emulator memory, typically located on a memory expansion board and which can be composed of bipolar DRAMs.

The signals in the circuit of Figure 3 have the following descriptions:-

RA[9:0]:	DRAM multiplexed address inputs.
IENABLE:	selects emulator enabled or disabled (production build option)

XENABLE:	selects external DRAM emulator enabled or disabled. From memory expansion board.
ROWOK, COLOK:	Internal latched row/col address ok for DRAM emulator.
PROMOE:	Enable for emulator logic buffers.
PROMOEZ:	Enable for external emulator memory.
DRAM OE 0/1)	
)	DRAM control lines.
DRAM WE 0/1)	
D[31:0]:	CPU data bus.

It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

CLAIMS:

1. A dynamic RAM emulator including a block of addressable memory and address control means arranged to address a selected word within the block, the address means including row and column latches for demultiplexing and latching a multiplexed address asserted on an address bus of a processor or a decoded memory selection signal derived from the multiplexed address, a data output arranged to be connected to a data bus of the processor and control logic to control latching of the address or memory selection signal, and to enable the data output, said logic also being arranged to override a data bus output enable of the processor and to enable or disable outputs of other memory devices connected to the data bus in accordance with the address latched in the address latch.

2. The dynamic RAM emulator of claim 1 wherein the block of addressable memory is implemented as a PROM.

3. The dynamic RAM emulator of claim 1 wherein the block of addressable memory is implemented as one or more logic buffer arrays, each array being one data word wide and each array having a hard coded input.

4. The dynamic RAM emulator of claim 3 wherein each logic buffer array input is provided by a switch.

5. The dynamic RAM emulator of claim 3 wherein the inputs of each logic buffer array are hard wired with logic levels representing an input code.

6. The dynamic RAM emulator as claimed in any one of claims 3, 4 or 5 wherein a single logic buffer array is coded as a jump relative instruction and the address decoding is arranged such that the single logic buffer array occupies a plurality of addresses.

7. The dynamic RAM emulator as claimed in any one of claims 1 to 6 wherein a plurality of low order address lines are demultiplexed to address discreet words in the address space of the block of addressable memory and the remaining address lines are demultiplexed and decoded to provide an enable signal for the dynamic RAM emulator.

8. The dynamic RAM emulator as claimed in any one of claims 3 to 6 wherein the address lines are demultiplexed and decoded to provide an enable signal for each array of logic buffers.

9. The dynamic RAM emulator as claimed in claim 8 wherein several addresses in the address space of the block of addressable memory are decoded to select a single array of logic buffers.

10. A slot machine having game playing means and control means wherein the control means includes memory means incorporating a dynamic RAM emulator including a block of addressable memory and address control means arranged to address a selected word within the block, the address means including row and column latches for demultiplexing and latching a multiplexed address asserted on an address but of a processor or a decoded memory selection signal derived from the multiplexed address, a data output arranged to be connected to a data bus of the processor and control logic to control latching of the address or memory selection signal, and to enable the data output, said logic also being arranged to override a data bus output enable of the processor and to enable or disable outputs of other memory devices connected to the data bus in accordance with the address latched in the address latch.

11. The slot machine of claim 10 wherein the block of addressable memory is implemented as a PROM.

12. The slot machine of claim 10 wherein the block of addressable memory is implemented as one or more logic buffer arrays, each array being one data word wide and each array having a hard coded input.

13. The slot machine of claim 12 wherein each logic buffer array input is provided by a switch.

14. The slot machine of claim 12 wherein the inputs of each logic buffer array are hard wired with logic levels representing an input code.

15. The slot machine as claimed in any one of claims 12, 13 or 14 wherein a single logic buffer array is coded as a jump relative instruction and the address decoding is arranged such that the single logic buffer array occupies a plurality of address.

16. The slot machine as claimed in any one of claims 10 to 15 wherein a plurality of low order address lines are demultiplexed to address discreet words in the address space of the block of addressable memory and the remaining address lines are demultiplexed and decoded to provide an enable signal for the dynamic RAM emulator.

17. The slot machine as claimed in any one of claims 12 to 15 wherein the address lines are demultiplexed and decoded to provide an enable signal for each array of logic buffers.

18. The slot machine as claimed in claim 17 wherein several addresses in the address space of the block of addressable memory are decoded to select a single array of logic buffers.

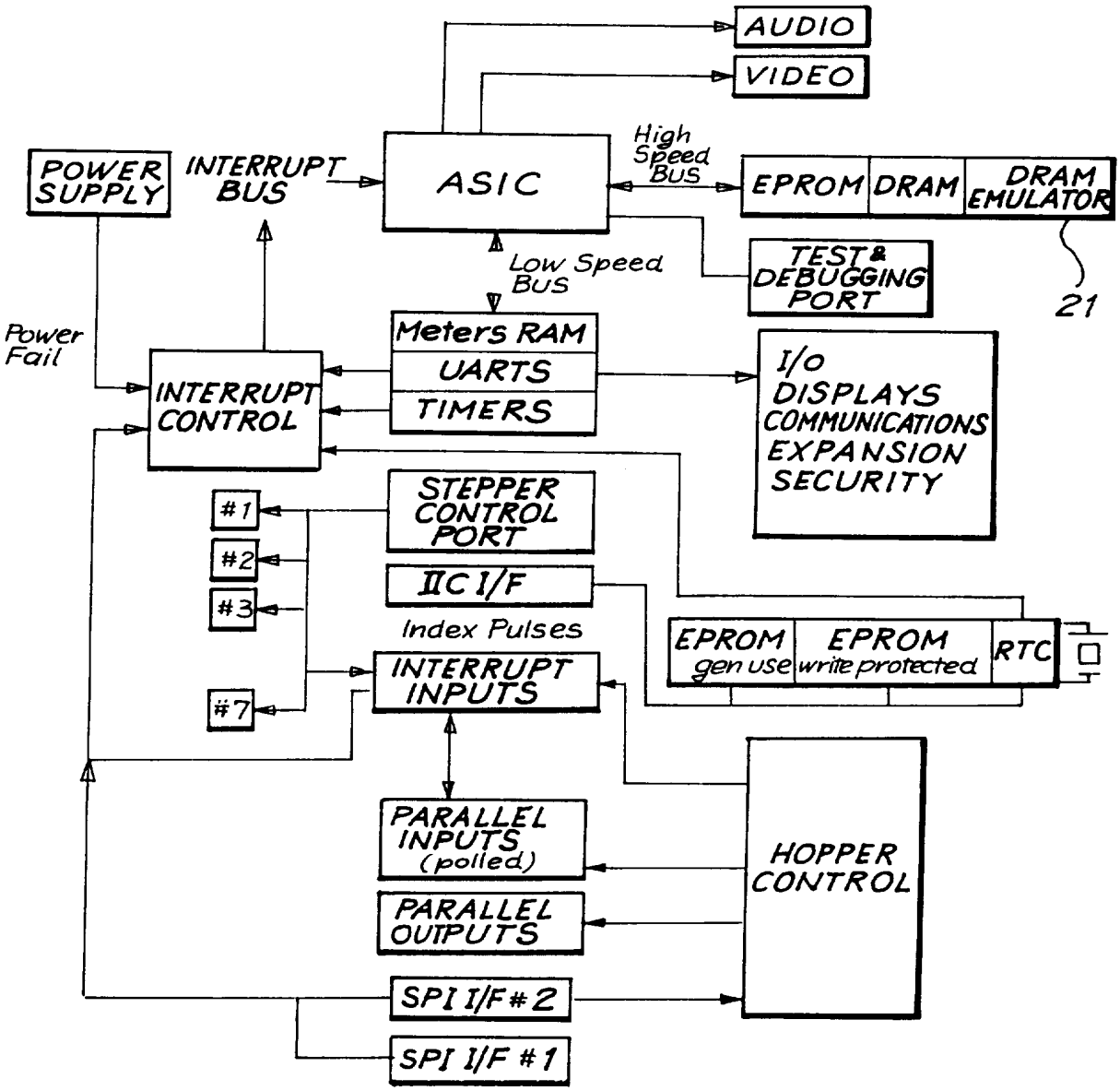
AUDIO
VIDEO
POWER SUPPLY
INTERRUPT BUS
ASIC
High Speed Bus
EPROM
DRAM
DRAM EMULATOR
TEST & DEBUGGING PORT
21
Low Speed Bus
Power Fail
Meters RAM
UARTS
TIMERS
INTERRUPT CONTROL
I/O
DISPLAYS
COMMUNICATIONS
EXPANSION
SECURITY
#1
#2
#3
#7
STEPPER CONTROL PORT
IIC I/F
Index Pulses
INTERRUPT INPUTS
EPROM gen use
EPROM write protected
RTC
PARALLEL INPUTS (polled)
PARALLEL OUTPUTS
HOPPER CONTROL
SPI I/F#2
SPI I/F #1

FIG. 1

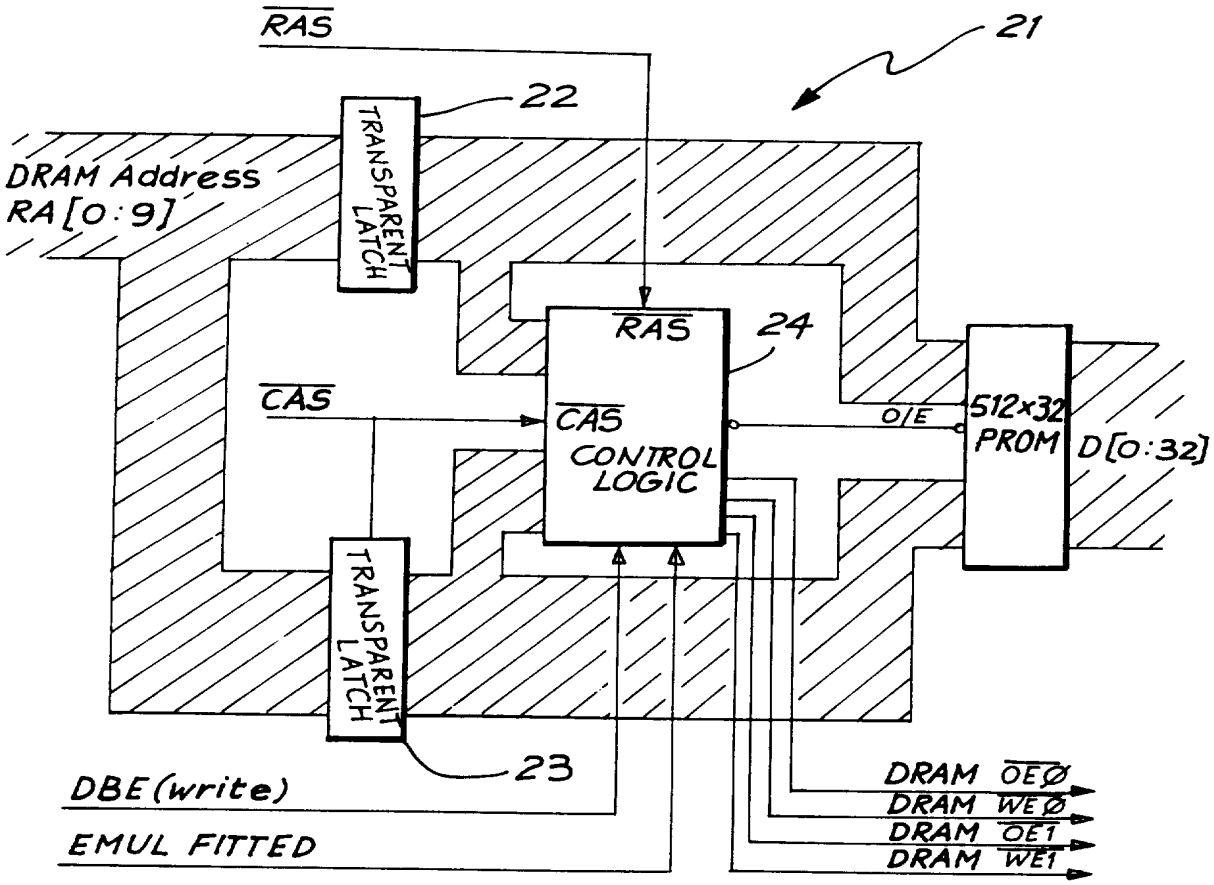
RAS
21
22
TRANSPARENT LATCH
DRAM Address
RA[0:9]
RAS
24
CAS
CAS
CONTROL LOGIC
O/E
512x32 PROM
D[0:32]
TRANSPARENT LATCH
23
DBE(write)
EMUL FITTED
DRAM OEØ
DRAM WEØ
DRAM OE1
DRAM WE1

FIG. 2

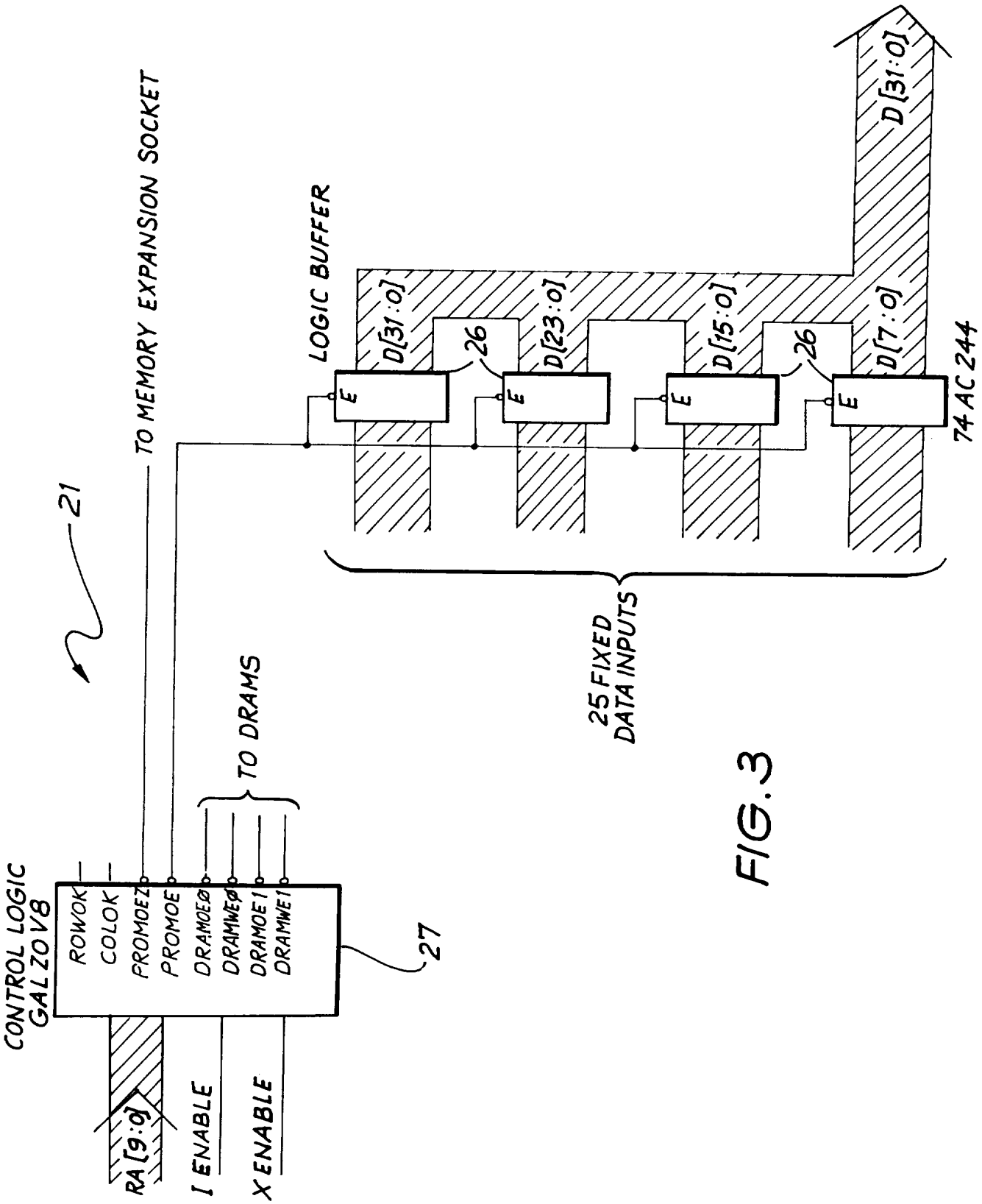
CONTROL LOGIC
GAL 20 V8
ROWOK
COLOK
PROMOEZ
PROMOE
DRAMOEØ
DRAMWEØ
DRAMOE1
DRAMWE1
27
21
TO MEMORY EXPANSION SOCKET
TO DRAMS
RA[9:0]
I ENABLE
X ENABLE
LOGIC BUFFER
D[31:0]
26
D[23:0]
D[15:0]
26
D[7:0]
D[31:0]
E
74 AC 244
25 FIXED
DATA INPUTS

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 96/00062

A. CLASSIFICATION OF SUBJECT MATTER

Int Cl[6]: G06F 12/14, 12/06, G11C 8/00, G07F 17/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC as above

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
AU : IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPAT, JAPIO, INSPEC (EMULAT: ROM, RAM, MEM)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 94/20906 (M-SYSTEMS LTD) 15 September 1994, Abstract	1
Y	US 5276843 (MICRON TECHNOLOGY) 4 January 1994, Whole document	1
Y	US 5003507 (SIMON JOHNSON) 26 March 1991, Whole document	1

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

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"&" document member of the same patent family

Date of the actual completion of the international search
11 March 1996

Date of mailing of the international search report
20TH MARCH 1996.

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INTERNATIONAL SEARCH REPORT

nternational Application No.
PCT/AU 96/00062

C (Continuation) **DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 93/02417 (QUARTERDECK OFFICE SYSTEMS) 4 February 1993 Whole document	
A	US 5136590 (JOHN FLUKE MFG.) 4 August 1992 Abstract, Figures	

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 96/00062

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
WO	9420906	AU	62699/94	CN	1098526	EP	688450
		FI	954235	IL	108766	US	5404485
		ZA	9401446				
US	5276843						
US	5003507						
WO	9302417	AU	23395/92	BR	9206286	EP	595880
		FI	940168	JP	6508952	NO	940148
		US	5237669	US	5367658		
US	5136590	CN	1045655	EP	370929	JP	2201549
		US	5136590				

END OF ANNEX

DERWENT-ACC-NO: 1996-384614

DERWENT-WEEK: 199918

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TITLE: Secure dynamic RAM emulator for slot machine includes addressable memory block and address controller demultiplexing and latching address asserted on address bus

INVENTOR: MUIR R L

PATENT-ASSIGNEE: ARISTOCRAT LEISURE IND PTY LTD [ARISN]

PRIORITY-DATA: 1995AU-001054 (February 10, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
WO 9624900 A1	August 15, 1996	EN
AU 9646144 A	August 27, 1996	EN
ZA 9601056 A	November 29, 1996	EN
DE 19681206 T	February 12, 1998	DE
AU 692670 B	June 11, 1998	EN
NZ 300871 A	March 29, 1999	EN

DESIGNATED-STATES: AU DE NZ US AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
WO1996024900A1	N/A	1996WO-AU00062	February 8, 1996
AU 9646144A	N/A	1996AU-046144	February 8, 1996
AU 692670B	N/A	1996AU-046144	February 8, 1996
DE 19681206T	N/A	1996DE-1081206	February 8, 1996
NZ 300871A	N/A	1996NZ-300871	February 8, 1996
DE 19681206T	N/A	1996WO-AU00062	February 8, 1996
NZ 300871A	N/A	1996WO-AU00062	February 8, 1996
ZA 9601056A	Based on	1996ZA-001056	February 9, 1996

INT-CL-CURRENT:

TYPE	IPC DATE
CIPS	G06F12/06 20060101
CIPS	G06F12/14 20060101
CIPS	G07F17/32 20060101
CIPS	G07F17/34 20060101
CIPS	G11C5/00 20060101
CIPS	G11C7/24 20060101
CIPS	G11C8/00 20060101

ABSTRACTED-PUB-NO: WO 9624900 A1

BASIC-ABSTRACT:

The emulator includes a block of addressable memory and an

address controller arranged to address a selected word within the

block. The address controller includes row and column latches for

demultiplexing and latching a multiplexed address asserted on an

address bus of a processor or a decoded memory selection signal

derived from the multiplexed address.

A data output is arranged to be connected to a processor data bus

and control logic controlling latching of the address or memory

selection signal and enable the data output. The logic is also

arranged to override a data bus output enable of the processor and

enable or disable outputs of other memory devices connected to

the data bus in accordance with the address latched in the

address latch.

ADVANTAGE - Provides speed required for video manipulation.

CHOSEN-DRAWING: Dwg.1/3

TITLE-TERMS: SECURE DYNAMIC RAM EMULATION SLOT MACHINE ADDRESS MEMORY BLOCK CONTROL DEMULTIPLEXER LATCH BUS

DERWENT-CLASS: T01 U13 U14 W04

EPI-CODES: T01-H01A; U13-C04B1A; U14-A03B4; U14-A08A; W04-X02A; W04-X02C;

SECONDARY-ACC-NO:

Non-CPI Secondary Accession Numbers: 1996-324101